ATTORNEY'S DOCKET NO: 200309970-1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Paul J Mantey
Serial No: 10/662,034
Filed: 09/12/2003
For: Communications Bus Transceiver

Examiner: Matthew D. Spittle
Art Unit: 2111

Mail Stop Amendment - By EFS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO OFFICE ACTION

In response to the Office Action mailed April 6, 2007, having a response due by July 6, 2007, the following amendments and remarks are respectfully submitted:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 18 of this paper.

Conclusions begin on page 23 of this paper.

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

Claim 1 (currently amended). A computer system comprising:

a system bus implemented in accordance with an Inter-IC bus specification;

a bus controller coupled to the system bus and to a~~n~~ first internal bus;

a send machine coupled between a host processor and the bus controller over a second internal bus; and

a first first-in first-out (FIFO) buffer coupled to the send machine, the first FIFO further coupled in parallel with the send machine between the host processor and the bus controller over the first internal bus but not over the system bus~~, the first FIFO not being coupled to the send machine over the internal bus~~.

Claim 2 (original). The computer system of claim 1, wherein the first FIFO buffer comprises means for receiving a plurality of bytes from the host processor without interrupting the host processor.

Claim 3 (previously presented). The computer system of claim 1, wherein:

the first FIFO buffer comprises means for receiving a plurality of bytes from the host processor; and

the send machine comprises means for transmitting the plurality of bytes over the system bus without interrupting the host processor.

Claim 4 (original). The computer system of claim 1, further comprising:

a receive machine coupled between the host processor and the bus controller; and

a second FIFO buffer coupled to the receive machine and coupled between the host processor and the bus controller.

Claim 5 (previously presented). The computer system of claim 4, wherein the receive machine comprises means for generating a message checksum for a message while the message is being received by the bus controller over the system bus.

Claim 6 (previously presented). The computer system of claim 1, further comprising:

means for receiving a message from the host processor;

means for attempting to send the message over the system bus to a target device;

means for determining whether the message was received without errors by the target device; and

retry means for attempting again to send the message over the system bus to the target device if it is determined that the message was not received without errors by the target device.

Claim 7 (previously presented). The computer system of claim 6, wherein the retry means comprises means for attempting again to send the message over the system bus to the target device without interrupting the host processor if it is determined that the message was not received without errors by the target device.

Claim 8 (previously presented). The computer system of claim 6, wherein the retry means comprises means for attempting again to send the message over the system bus to the target device without obtaining the message again from the host processor if it is determined that the message was not received without errors by the target device.

Claim 9 (previously presented). The computer system of claim 1, further comprising:

busfree count means for storing a busfree count associated with the computer system;

a busfree timer for use by the computer system to wait an amount of time specified by the busfree count prior to attempting to access the system bus after the system bus becomes available for use; and

a fair arbitration block coupled between the host processor and the bus controller, the fair arbitration block comprising arbitration means for modifying the busfree count according to a priority signal to produce an arbitrated busfree count signal.

Claim 10 (original). The computer system of claim 1, further comprising:

a byte timer coupled between the bus controller and the host processor.

Claim 11 (previously presented). The computer system of claim 10, wherein the byte timer comprises means for determining whether the host processor has failed and means for generating a signal indicating whether the host processor has failed.

Claim 12 (currently amended). A computer system comprising:

a system bus implemented in accordance with an Inter-IC bus specification;

a bus controller coupled to the system bus and to a first internal bus and a second internal bus;

a send machine coupled between a host processor and the bus controller over the second internal bus, the send machine comprising means for transmitting the plurality of bytes over the system bus without interrupting the host processor;

a first first-in first-out (FIFO) buffer coupled to the send machine, the first FIFO further coupled in parallel with the send machine between the host processor and the bus controller over the first internal bus but not over the system bus, ~~the first FIFO not being coupled to the send machine over the first internal bus,~~ the first FIFO comprising means for receiving a plurality of bytes from the host processor without interrupting the host processor;

a receive machine coupled between the host processor and the bus controller, the receive machine comprising means for receiving the plurality of bytes over the system bus without interrupting the host processor; and

a second FIFO buffer coupled to the receive machine, the second FIFO further coupled between the host processor and the bus controller over the second internal bus, the second FIFO not being coupled to the receive machine over the second internal bus but not over the system bus, the second FIFO buffer comprising means for receiving a plurality of bytes from the bus controller without interrupting the host processor.

Claim 13 (previously presented). The computer system of claim 12, further comprising:

means for receiving a message from the host processor;

means for attempting to send the message over the system bus to a target device;

means for determining whether the message was received without errors by the target device;

retry means for attempting again to send the message over the system bus to the target device without interrupting the host processor if it is determined that the message was not received without errors by the target device;

busfree count means for storing a busfree count associated with the computer system;

a busfree timer for use by the computer system to wait an amount of time specified by the busfree count prior to attempting to access the system bus after the system bus becomes available for use;

a fair arbitration block coupled between the host processor and the bus controller, the fair arbitration block comprising arbitration means for modifying the busfree count according to a priority signal to produce an arbitrated busfree count signal; and

a byte timer coupled between the bus controller and the host processor, the byte timer comprising means for determining whether the host processor has failed and means for generating a signal indicating whether the host processor has failed.

Claims 14-41 (canceled).

Claim 42 (currently amended). A computer system comprising:

a system bus;

a bus controller coupled to the system bus and to ~~an~~ first internal bus;

a send machine coupled between a host processor and the bus controller over a second internal bus, the send machine comprising means for transmitting the plurality of bytes over the system bus without interrupting the host processor;

a first first-in first-out (FIFO) buffer coupled to the send machine, the first FIFO further coupled in parallel with the send machine between the host processor and the bus controller over the first internal bus but not over the system bus, ~~the first FIFO not being coupled to the send machine over the first internal bus,~~ the first FIFO comprising means for receiving a plurality of bytes from the host processor without interrupting the host processor;

a receive machine coupled between the host processor and the bus controller, the receive machine comprising means for receiving the plurality of bytes over the system bus without interrupting the host processor;

a second FIFO buffer coupled to the receive machine, the second FIFO further coupled between the host processor and the bus controller over the second internal bus but not over the system bus, the second FIFO not being coupled to the receive machine over the second internal bus, the second FIFO buffer comprising means for receiving a plurality of bytes from the bus controller without interrupting the host processor;

means for receiving a message from the host processor;

means for attempting to send the message over the system bus to a target device;

means for determining whether the message was received without errors by the target device;

retry means for attempting again to send the message over the system bus to the target device without interrupting the host processor if it is determined that the message was not received without errors by the target device;

busfree count means for storing a busfree count associated with the computer system;

a busfree timer for use by the computer system to wait an amount of time specified by the busfree count prior to attempting to access the system bus after the system bus becomes available for use;

a fair arbitration block coupled between the host processor and the bus controller, the fair arbitration block comprising arbitration means for modifying the busfree count according to a priority signal to produce an arbitrated busfree count signal; and

a byte timer coupled between the bus controller and the host processor, the byte timer comprising means for determining whether the host processor has failed and means for generating a signal indicating whether the host processor has failed.

Claim 43 (currently amended). A computer system comprising:

a system bus;

a bus controller coupled to the system bus and to a first internal bus and a second internal bus;

a send machine coupled between a host processor and the bus controller over the second internal bus, the send machine comprising means for transmitting the plurality of bytes over the system bus without interrupting the host processor;

a first first-in first-out (FIFO) buffer coupled to the send machine, the first FIFO further coupled in parallel with the send machine between the host processor and the bus controller over the first internal bus but not over the system bus, ~~the first FIFO not being coupled to the send machine over the first internal bus,~~ the first FIFO comprising means for receiving a plurality of bytes from the host processor without interrupting the host processor;

a receive machine coupled between the host processor and the bus controller, the receive machine comprising means for receiving the plurality of bytes over the system bus without interrupting the host processor and means for generating a message checksum for a message while the message is being received by the bus controller over the system bus without interrupting the host processor; and

a second FIFO buffer coupled to the receive machine, the second FIFO further coupled between the host processor and the bus controller over the second internal bus but not over the system bus, the second FIFO not being coupled to the receive machine over the second internal bus, the second FIFO buffer comprising means for receiving a plurality of bytes from the bus controller without interrupting the host processor.

Claim 44 (currently amended). A device for use in a computer system including a system bus and a bus controller coupled to the system bus and to a first internal bus and a second internal bus, the device comprising:

a send machine coupled between a host processor and the bus controller over a second internal bus, the send machine comprising means for transmitting the plurality of bytes over the system bus without interrupting the host processor;

a first first-in first-out (FIFO) buffer coupled to the send machine, the first FIFO further coupled in parallel with the send machine between the host processor and the bus controller over the first internal bus but not over the system bus, ~~the first FIFO not being coupled to the send machine over the first internal bus,~~ the first FIFO comprising means for receiving a plurality of bytes from the host processor without interrupting the host processor;

a receive machine coupled between the host processor and the bus controller, the receive machine comprising means for receiving the plurality of bytes over the system bus without interrupting the host processor;

a second FIFO buffer coupled to the receive machine, the first FIFO further coupled between the host processor and the bus controller over the second internal bus but not over the system bus, the second FIFO not being coupled to the receive machine over the second internal bus, the second FIFO buffer comprising means for receiving a plurality of bytes from the bus controller without interrupting the host processor;

busfree count storage means for storing a busfree count associated with the computer system;

a busfree timer for use by the computer system to wait an amount of time specified by the busfree count prior to attempting to access the system bus after the system bus becomes available for use; and

a fair arbitration block coupled between the host processor and the bus controller, the fair arbitration block comprising arbitration means for modifying the busfree count according to a priority signal to produce an arbitrated busfree count signal.

REMARKS/ARGUMENTS

Interview Summary

Applicant thanks the Examiner for extending the courtesy of a telephonic interview on June 18, 2007. In that interview, the Examiner suggested amending the claims to clarify which "internal bus" the bus controller is connected to. Applicant's Attorney agreed to make such clarifying amendment(s). The Examiner agreed that either of Applicant's proposals to amend claim 1 would distinguish claim 1 over the cited references, namely amendments which would clarify that: (1) the send machine is coupled between the host processor and the bus over a path that is distinct from the path between the FIFO and the host processor; or (2) the send machine and FIFO are connected in parallel with respect to the bus controller and host processor. No final agreement was reached regarding the allowability of the claims in light of any such amendments.

Claim Status

Claims 1-13 and 42-44 are pending in this application. Claims 1-13 and 42-44 stand rejected.

Claims 1, 12, and 42-44 have been amended. No claims have been canceled or added.

Claim Rejections – 35 U.S.C. § 102

Claims 1-4, 12, and 43 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Johnson et al. (U.S. Pat. No. 6,122,758). Applicant traverses this rejection and respectfully requests that it be withdrawn in light of the amendments made herein.

Claim 1, for example, has been amended to recite that the first FIFO is coupled *in parallel with the send machine* between the host processor and the bus controller over the first internal bus but not over the system bus. Support for this amendment may be found, for example, at FIG. 2A (and accompanying text), which illustrates FIFO 288 coupled in parallel with send machine 210 between the host processor 238 and the bus controller 208. Furthermore, FIFO 288 is shown as being coupled over an internal bus consisting of buses 252 and 216.

Johnson does not disclose these limitations of claim 1, as amended. For example, even if the request queue 516 shown in FIG. 7 of Johnson is interpreted as a "first FIFO," the MDF 707 is interpreted as a "send machine," the system interface processor 312 is interpreted as a "bus controller," the microcontroller bus 310 is interpreted as a "system bus," and the ISA bus 226 is interpreted as an "internal bus," the request queue 516 and send machine 707 of Johnson are coupled *serially* between the system interface processor

312 and the ISA bus 226, not *in parallel*, as required by claim 1, as amended.

Claim 1 has been further amended to clarify that the bus controller is coupled to the system bus and to a first internal bus. An example of the first internal bus in FIG. 2A of the present application is the bus consisting of buses 252 and 216. Claim 1 has been further amended to clarify that the send machine is coupled between the host processor and the bus controller over a second internal bus, an example of which is the bus consisting of lines 212, 254, and 256 in FIG. 2A of the present application.

Claim 1 has been further amended to remove the limitation of "the first FIFO not being coupled to the send machine over the internal bus," since the newly added limitation that the first FIFO is coupled in parallel with the send machine sufficiently clarifies the connections among the elements of claim 1 to distinguish over the cited references.

For at least these reasons, claim 1 patentably distinguishes over Johnson. Claims 2-4 depend from claim 1 and therefore patentably distinguish over Johnson for at least the same reasons as claim 1.

Independent claims 12 and 43 have been amended to include substantially the same relevant limitations as claim 1 and therefore

patentably distinguish over Johnson for at least the same reasons as claim 1.

Claim Rejections – 35 U.S.C. § 103

Claims 5, 6-8, 9, 10-11, 13, 42, and 44 stand rejected over Johnson in view of various other previously-cited references. Neither Johnson nor any of these other references, either singly or in combination, teaches or suggests the above-mentioned requirement that the first FIFO be coupled in parallel with the send machine between the host processor and the bus controller.

Claims 5, 6-8, 9, and 10-11 depend, either directly or indirectly, from claim 1 and therefore include at least the same limitations as claim 1. Claims 5, 6-8, 9, and 10-11, therefore, patentably distinguish over the cited combinations for at least the reasons provided above with respect to claim 1.

Claim 13 depends, either directly or indirectly, from claim 12 and therefore includes at least the same limitations as claim 12. Claim 13, therefore, patentably distinguishes over the cited combinations for at least the reasons provided above with respect to claim 12.

Claim 42 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Johnson in view of Feeney, Cao, and Webb. Neither Johnson nor any of these other references, either singly or in

combination, teaches or suggests the above-mentioned requirement that the first FIFO be coupled in parallel with the send machine between the host processor and the bus controller. Claim 42 has been amended to include substantially the same relevant limitations as claim 1 and therefore patentably distinguishes over the cited combination for at least the same reason.

Claim 44 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Johnson in view of Cao. Neither Johnson nor Cao, either singly or in combination, teaches or suggests the above-mentioned requirement that the first FIFO be coupled in parallel with the send machine between the host processor and the bus controller. Claim 44 has been amended to include substantially the same relevant limitations as claim 1 and therefore patentably distinguishes over the cited combination for at least the same reason.

CONCLUSIONS

Any dependent claims not specifically discussed above depend, either directly or indirectly, from the independent claims discussed above and therefore are patentable for at least the same reason(s).

If the Examiner wishes to discuss this Response, the Examiner is requested to call the Applicant's attorney at the phone number listed below.

If this response is not considered timely filed and if a request for extension of time is otherwise absent, applicant hereby requests any extension of time. Please charge any fees or make any credits, to Deposit Account No. 08-2025.

Respectfully submitted,

/Robert Plotkin/ June 21, 2007
Robert Plotkin, Esq. Date
Reg. No. 43,861

Robert Plotkin, P.C.
35 Corporate Drive, 4th Floor
Burlington, MA 01803
Tel: (978) 318-9914
Fax: (978) 318-9060